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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,687	04/07/2007	Spartak Gevorgian	0110-095	9509

42015 7590 09/02/2008

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EXAMINER	
STEVENS, GERALD D	

ART UNIT	PAPER NUMBER
2817	

NOTIFICATION DATE	DELIVERY MODE
09/02/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/596,687	GEVORGIAN ET AL.	
	Examiner	Art Unit	
	GERALD STEVENS	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-51 and 53-55* is/are rejected.

7)☒ Claim(s) *52 and 56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/21/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 29,32,34,40,43,44 provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1,6,11 of copending Application No. 11/543,655 in view of Kai et al (US 2002/0187902).

Regarding claims 29,32,34,40,43, & 44, the copending application, as described in the limitations of the claims, teaches having a frequency selective filter comprising: a substrate, a patterned (i.e. **claim 34**) bottom metal layer (i.e. a second metal layer) deposited on said substrate, a ferroelectric thin film that is deposited on said bottom metal layer (i.e. **claim 32**, wherein the ferroelectric is unpatterned), and a top metal (i.e. first metal layer) electrode deposited on said ferroelectric thin film. The top metal

electrode is patterned to form a coplanar waveguide transmission line, but fails to teach having a microwave device.

Kai, as depicted in fig. 2b, teaches having a flat circuit body (30) comprising: two ground layers (33-1 & 33-2) that are disposed longitudinally on both sides of a signal transmission line (32). The signal transmission line (32) is made of a known microstrip line (i.e. **claim 40**) in a known coplanar waveguide (i.e. **claim 44**) configuration to pass signals in the microwave band (i.e. a microwave device, wherein the signal transmission line passes the microwave signal and is therefore a microwave transmission line, i.e. **claim 43**).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have replaced the coplanar waveguide such as taught by the copending application with the coplanar waveguide such as taught by Kai because it is obvious to have used a specific art equivalent coplanar waveguide such as taught by Kai in the place of the art equivalent generic coplanar waveguide such as taught by the copending application.

This is a provisional obviousness-type double patenting rejection.

2. Claims 29,30,32,33,35,36,43-45 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1,9,13,14,18,26,30,31 of U.S. Patent No. 7030463. Although the conflicting claims are not identical, they are not patentably distinct from each other because the prior related U.S. patent, as described in claims 1 & 18, teaches having an electrically tunable

electromagnetic band gap structure (i.e. **claim 30**) comprising: a semiconductive (i.e. **claim 45**) substrate having an oxide layer and a generally planar surface, a signal strip (i.e. unpatterned second metal layer, i.e. **claim 33**) provided on the generally planar surface of the oxide layer, a tunable ferroelectric layer (i.e. unpatterned ferroelectric film layer, i.e. **claim 32**), a patterned metal layer (i.e. first metal layer) having ground lines and an electrode (i.e. transmission line) on a surface of the tunable ferroelectric layer, said ground lines and said electrode being separated by a gap and said signal strip and said electrode being separated by the tunable ferroelectric layer provided therebetween. Although claims 1 & 18 fail to teach the patterned metal layer (i.e. first metal layer) with the ground lines and electrode being a microwave device, claims 14 & 31 further describe the electrically tunable electromagnetic bandgap structure as being provided in a monolithic microwave integrated circuit, therefore it is obvious that the patterned metal layer with the ground lines and electrode is a microwave device and that the electrode (i.e. transmission line) passes microwave signals (i.e. a microwave transmission line, i.e. **claim 43**).

Also, claims 9, 26, 13, & 30, teach having a ferroelectric layer comprising Barium-Strontium Titanate, $Ba_XSr_{1-X}TiO_3$ (BSTO), where x can range from zero to one (i.e. **claim 36**) as described in claims 9 & 26 and having the signal strip and the electrode comprising platinum, gold, copper, silver, aluminum, other Periodic Table Group I, III, and VIII elements, and combinations thereof (i.e. **claim 35**), as discussed in claims 13 & 30.

Claim Rejections - 35 USC § 102

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 29, 46, & 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Subramanyam et al. (US 7030463)

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 29, 46, & 47, Subramanyam, as depicted in fig. 8B, exemplarily teaches having a micro strip circuit comprising: a substrate (49) with a patterned bottom electrode (44, i.e. first metal layer) disposed on top of it. Disposed upon the electrode (44) is a ferroelectric film (43) that has a patterned top electrode layer (42, i.e.

second metal layer) disposed upon it. Disposed above the top electrode layer (42) is a dielectric film made of BCB (i.e. **claims 46 & 47**) that has a patch radiator (i.e. microwave circuit device) disposed upon it.

2. Claims 29, 32, 34-36, 43-45, 50, & 51 are rejected under 35 U.S.C. 102(e) as being anticipated by Subramanyam et al. (US 20070024400)

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 29,32, 34-36,43-45, 50, & 51, Subramanyam, as depicted in fig. 1, exemplarily teaches having a capacitive shunt switch that is used as a semiconductor diode in a monolithic microwave integrated circuit (MMIC, pg. 1 background of the invention par. 2-3, i.e. **claim 51**) comprising: A substrate made of two layers that are composed of high resistivity silicon (40) and a layer of silicon oxide (35, i.e. a dielectric, i.e. **claim 45**). Disposed above the substrate is an unpatterned (pg. 1 par. 0009, i.e. **claim 32**) ferroelectric thin-film (20, i.e. layer of a ground plane structure) layer, that is 100-400 nm thick (pg. 2 par. 0036, i.e. **claim 50**) and is made of barium strontium titanate (pg. 3 par. 0037, i.e. **claim 36**), that is sandwiched between a layer of patterned (pg. 3 par. 0037) platinum/gold (25, i.e. a second metal layer of

ground plane structure) and a layer of gold (15, i.e. first metal layer of ground plane structure, i.e. the platinum/gold, gold, and ferroelectric thin-film layers make up the layered ground plane structure). The layer of patterned platinum/gold (25) is a part of an electromagnetic band gap structure (i.e. **claims 30, 35**) that is disposed below the ferroelectric-thin film (20) and is attached to the substrate via a titanium adhesion layer (30). The layer of gold (15) is disposed above the ferroelectric-thin film (20) and has a coplanar waveguide (CPW) transmission line (10, i.e. a microwave circuit device, i.e. **claims 43, 44**) disposed above it. More specifically, as shown in fig. 2d, the layer of gold (15) is patterned (i.e. **claim 34**) to form a central signal strip (100) and ground conductors (110) on its top surface to form the CPW (10), see pg. 3 par. 0038 (wherein fig. 2b is the same embodiment).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanyam.

Regarding claims 40-42, Subramanyam teaches all of the elements as discussed above in claim 29, but fails to teach the microwave circuit device comprising a patch resonator, at least one micro stripline, and an inductor coil.

Although Subramanyam fails to teach the microwave circuit device comprising a patch resonator, at least one micro stripline, and an inductor coil, it is well known in the art that such devices are used for filtering means with a ferroelectric.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to have replaced the coplanar waveguide transmission line such as taught by Subramanyam with the micro stripline, inductor coil, or patch resonator such as well known in the art because they provide the benefit of providing filtering means for a signal. For example, see Fiedziuszko et al (fig. 2 four pole patch filter), Toncich (fig. 2 micro strip resonator), and Brommer et al (fig. 9 tunable filter).

5. Claims 31, 33, 37-39, 48, 49, 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanyam et al in view of Hunt et al.

Regarding claim 31, Subramanyam teaches all of the elements as discussed above in claim 29, but fails to teach having a patterned ferroelectric film layer.

Hunt, as depicted in fig. 13, teaches having an electrically adjustable capacitor with an alternative form of the dielectric electrode structure comprising a patterned dielectric (i.e. ferroelectric, col. 15 lines 33-36).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have replaced the ferroelectric layer such as taught by Subramanyam with the patterned ferroelectric such as taught by Hunt because patterned ferroelectric such as taught by Hunt provides the benefit of reducing the problems of adhesion between the conductors and the dielectric layer (col. 15 lines 33-36).

Regarding claim 33, Subramanyam teaches all of the elements as discussed above in claim 29, but fails to teach having a second metal layer that is not patterned.

Hunt, as depicted in fig. 6, teaches having a biasing electrode (62, i.e. a second metal layer) that is not patterned after being disposed on a supporting substrate (61, col. 9 lines 56-58).

It would have been obvious to one having ordinary skill in the art at the time of the invention to have replaced the patterned gold layer such as taught by Subramanyam with the unpatterned biasing electrode such as taught by Hunt (fig. 6) because it is obvious to have used an art equivalent unpatterned biasing electrode such as taught by Hunt in the place of art equivalent patterned electrode such as taught by Subramanyam.

Regarding claims 37-39, 48, 49, Subramanyam teaches all of the elements as discussed above in claim 29, but fails to teach having the layered ground plane structure being tunable in response to a DC voltage being applied between the first patterned metal layer and the second metal layer.

Hunt, as depicted in fig. 6, exemplarily teaches having an electrically adjustable capacitor comprising: a supporting substrate (61) that has a first biasing electrode (62 i.e. layer of a ground plane structure) that is directly connected to a highly conductive line (68 i.e. RF electrode). On top of the first biasing electrode (62) is a ferroelectric layer (64, i.e. layer of a ground plane structure) and disposed on top of the ferroelectric layer (64) is a second biasing electrode (66, i.e. layer of a ground plane structure) that is directly connected to another highly conductive line (67 i.e. RF electrode). Through the

direct connection (i.e. no decoupling circuits) of the highly conductive lines (67, 68, i.e. RF electrodes) a DC voltage, that can be even less than 3 volts, is applied to the first (62) and second (66) biasing electrodes (i.e. protrusions) to charge them up to the DC voltage level (col. 6 lines 24-28). This charging of the first (62) and second (66) biasing electrodes allows for the biasing of the ferroelectric layer (64). Also, although it is not explicitly stated in the reference, it is obvious that tuning the ferroelectric layer (64) through the application of a DC voltage will tune the highly conductive lines (67, 68, i.e. microwave circuit device) and it is obvious that the DC voltage applied to the first and second biasing electrodes (62,66) affects their dielectric constants, thereby changing the impedance of the biasing electrodes (62,66, i.e. layers of a ground plane structure) that are adjacent to the highly conductive lines (67,68, i.e. microwave circuit device). It would have been obvious to one having ordinary skill in the art at the time of the invention to have added the DC bias voltage such as taught by Hunt to the gold metal layers such as taught by Subramanyam because the DC bias voltage such as disclosed by Hunt provides the benefit of tuning the capacitance of the adjustable capacitor, as known to those of ordinary skill in the art.

Also, as an obvious consequence of the combination, a DC voltage, that can be even less than 3 volts (i.e. **claims 48, 49**), is directly connected (i.e. no decoupling components) to the gold (i.e. first metal layer) and platinum/gold (i.e. second metal layer) layers of the capacitive shunt switch and therefore, the dielectric constants of the gold and platinum/gold layers change, thereby changing the impedance of the platinum/gold and gold layers (i.e. ground plane structure). This change in impedance

tunes the CPW (i.e. microwave circuit), which is adjacent to one of the gold layer (i.e. first metal layer, i.e. **claims 37-39**).

Regarding claims 53-55, Subramanyam, as depicted in fig. 1, exemplarily teaches having a capacitive shunt switch comprising: A substrate made of two layers that are composed of high resistivity silicon (40) and a layer of silicon oxide (35). Disposed above the substrate is a ferroelectric thin-film (20, i.e. layer of a ground plane structure) layer that is sandwiched between a layer of patterned (pg. 3 par. 0037) platinum/gold (25, i.e. a second metal layer of ground plane structure) and a layer of gold (15, i.e. first metal layer of ground plane structure, i.e. the platinum/gold, gold, and ferroelectric thin-film layers make up the layered ground plane structure). The layer of patterned platinum/gold (25) is a part of an electromagnetic band gap structure (i.e. **claim 54**) that is disposed below the ferroelectric-thin film (20) and is attached to the substrate via a titanium adhesion layer (30). The layer of gold (15) is disposed above the ferroelectric-thin film (20) and has a coplanar waveguide (CPW) transmission line (10, i.e. a microwave circuit device) disposed above it. More specifically, as shown in fig. 2d, the layer of gold (15) is patterned to form a central signal strip (100) and ground conductors (110) on its top surface to form the CPW (10), see pg. 3 par. 0038 (wherein fig. 2b is the same embodiment).

Hunt, as depicted in fig. 6, exemplarily teaches having an electrically adjustable capacitor comprising: a supporting substrate (61) that has a first biasing electrode (62 i.e. layer of a ground plane structure) that is directly connected to a highly conductive

line (68 i.e. RF electrode). On top of the first biasing electrode (62) is a ferroelectric layer (64, i.e. layer of a ground plane structure) and disposed on top of the ferroelectric layer (64) is a second biasing electrode (66, i.e. layer of a ground plane structure) that is directly connected to another highly conductive line (67 i.e. RF electrode). Through the direct connection (i.e. no decoupling circuits) of the highly conductive lines (67, 68, i.e. RF electrodes) a DC voltage is applied to the first (62) and second (66) biasing electrodes (i.e. protrusions) to charge them up to the DC voltage level (col. 6 lines 24-28). This charging of the first (62) and second (66) biasing electrodes allows for the biasing of the ferroelectric layer. Also, although it is not explicitly stated in the reference, it is obvious that tuning the ferroelectric layer (64) through the application of a DC voltage will tune the highly conductive lines (67, 68, i.e. microwave circuit device) and it is obvious that the DC voltage applied to the first and second biasing electrodes (62,66) affects their dielectric constants, thereby changing the impedance of the biasing electrodes (62,66, i.e. layers of a ground plane structure) that are adjacent to the highly conductive lines (67,68, i.e. microwave circuit device) and changing the resonant frequency of the highly conductive lines (67,68, i.e. microwave circuit device).
It would have been obvious to one having ordinary skill in the art at the time of the invention to have added the DC bias voltage such as taught by Hunt to the gold metal layers such as taught by Subramanyam because the DC bias voltage such as disclosed by Hunt provides the benefit of tuning the capacitance of the adjustable capacitor, as known to those of ordinary skill in the art.

Furthermore, as an obvious consequence of the above combination, a DC voltage is attached to the gold (i.e. first metal layer) and platinum/gold (i.e. second metal layer) layers of the capacitive shunt switch and therefore, the dielectric constants of the gold and platinum/gold layers change, thereby changing the impedance of the platinum/gold and gold layers (i.e. ground plane structure) and changing the resonant frequency of the CPW (i.e. microwave circuit, i.e. **claim 55**).

Allowable Subject Matter

6. Claims 52, 56 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GERALD STEVENS whose telephone number is (571)270-5076. The examiner can normally be reached on Mon-Fri 7:30am - 5:00pm EST alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BENNY LEE/
PRIMARY EXAMINER
ART UNIT 2817

GDS